CLAIMS

What is claimed is:

1. A semiconductor memory device comprising:

a sense line;

a data line;

a memory connected between the sense line and the data line having an active restoration function; and

a sense amplifier connected between the sense line and the data line, which senses and inverts data on the sense line, and outputs inverted data to the data line;

wherein data on the sense line is of a polarity that is opposite that of data on the data line, and wherein the data on the data line are written to the memory.

2. The semiconductor memory device of claim 1, wherein the memory having the active restoration function includes a storage node having a gate of a transistor formed on a semiconductor substrate, wherein the data line is formed on the storage node, wherein a word line is formed on the data line, and wherein charge on the data line is transferred to the storage node or discharged from the storage node in response to a voltage of the word line.

3. The semiconductor memory device of claim 1, wherein the data stored in the memory having the active restoration function is read from the sense line in response to a first voltage which is supplied to the word line of the memory having the active restoration function, and wherein the data in the data line are written into the storage node of the memory having the restoration function in response to a second voltage which is supplied to the word line.

4. The semiconductor memory device of claim 3, wherein the first voltage is lower than the second voltage.

5. The semiconductor memory device of claim 1, wherein the memory having the active restoration function is a scalable two-transistor memory.

6. A semiconductor memory device having an active restoration function, the semiconductor memory device comprising:

a sense line which carries sense data read from the memory having the active restoration function;

a data line connected to the memory having the active restoration function; and

an inverting sense amplifier connected between the sense line and the data line, which senses and inverts the sense data on the sense line, which outputs inverted data to the data line, and which senses and inverts data on the bit line and outputs inverted data to the sense line;

wherein data on the data line are written to the memory having the active restoration function.

7. The semiconductor memory device of claim 6, wherein the data stored in the memory having the active restoration function are read from the bit line in response to a first voltage which is supplied to the word line of the memory having the active restoration function, and wherein the data in the data line are written to the memory having the active restoration memory in response to a second voltage which is supplied to the word line.

8. A semiconductor memory device comprising:

a first block which has a first bit line, a first data line, and a memory having a first active restoration function that is connected between the first bit line and the first data line;

a second block which has a second bit line, a second data line, and a memory having a second active restoration function that is connected between the second bit line and the second data line; and

an inverting sense amplifier which is laid out between the first block and the second block and connected between the first bit line and the first data line;

wherein a first bit line is connected to the second data line through the inverting sense amplifier and wherein the first data line is connected to the second bit line through the inverting sense amplifier, and

wherein a polarity of the data in each bit line is opposite to the polarity of the data in each data line and the data in each data line are written to the corresponding memory having the first active restoration function or the second active restoration function.

9. A semiconductor memory device comprising:

a bit line;

a data line;

a memory connected between the bit line and the data line, the memory having an active restoration function; and

an inverting circuit connected between the bit line and the data line;

wherein data on the data line is of a polarity that is opposite that of data on the bit line.

10. The semiconductor memory device of claim 9, wherein the memory having the active restoration function and the inverting circuit constitutes a latch loop.

11. A semiconductor memory device comprising;

a bit line;

a first switching circuit connected between a first voltage and the bit line that switches the bit line to the first voltage in response to a control signal;

a data line;

a second switching circuit connected between a second voltage and the data line that switches the data line to the second voltage in response to the control signal;

a memory connected between the bit line and the data line, the memory having an active restoration function; and

a third switching circuit connected between a third voltage and the data line that connects the third voltage to the data line in response to a voltage of the bit line.

12. The semiconductor memory device of claim 11, wherein the memory having the active restoration function and the third switching circuit constitute a latch.

13. The semiconductor memory device of claim 11, wherein the data in the data line are written to the memory having the active restoration function.